Common Mistakes by Authors in Listing References

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Reference is a *list of the sources* we have cited during our research. To write our own work in a related field is one of the essential parts of the research writing. Every source listed in our references should be accessible by others who read our work.This is achieved by citing related work within the text and by listing all cited references at the end of the paper. Different publishers require different formats for citing a paper in the text and for listing references. Regardless of the citation style, there are two basic rules for the list of references: (1) Every cited source must be listed and (2) Every listed source must be cited.
To write any publications, authors have no other choice than adhering to the style required by publishers but mostly who belongs to IEEE publishers require to use almost same referencing styles. However we come across general/common mistakes made by authors in listing references.

Section I: Comparison between Incorrect and Correct References

Incorrect References

[1] M. H. Na, E. J. Nowak, W. Haensch and J. Cai, "The effective drive current in CMOS inverters," *in Proc. Int. Electron Devices Meeting (IEDM)*, Dec. 2002, pp. 541–544. (Remark: 1)

[2] D. Chang, M. Lee, D. Chen, and V. Liva, "Power Junction FETs (JFETs) For Very Low-Voltage Applications,"*in Proc. IEEE Applied Power Electronics Conference Exposition (APEC)*, vol. 3, no. 8, 2005, pp. 1419–1423. (Remark: 2)

[3] Mayank Kumar, Mukesh Kumar, Anil Kumar, Ashish Das, A.K.Jaiswal, Gaurav Nigam, and Kamal Prakash Pandey, "An improved device consideration for ultra-low power applications in junction field effect transistor," *International Journal of Emerging Technology and Advanced Engineering (IJETAC)*, vol. 3,Issue: 2, Feb. 2013. (Remark: 3)

[4] S. Ono, Y. Yamaguchi, Y. Kawaguchi, and A. Nakagawa, "30 V sub-micron shallow junction planar-MOSFET for DC–DC converters," *in Proc. Int. Symp. Power Semicond. Devices ICs (ISPSD)*, Japan, 2004, pp. 401-404. (Remark: 4)

[5] T V Meenu, and Rama Komaragiri, "A vertical JFET with improved on to off current performance," *IEEE International Conference on Microelectronics, Communications and Renewable Energy (ICMiCR)*, pp.1-5, June 2013. (Remark: 5)

[6] Chun Chiang, Ping-Chen Chang, Pei-Shan Tseng, Po-Ya Lai, Tien-Hao Tang, and Kuan-Cheng Su, "Optimization of PESD implant design for ESD robustness of 5V drain-back N-LDMOSFET," *IEEE International Reliability Physics Symposium* , 2016, pp. EL-31–EL-34. (Remark: 6)

[7] C-Wei Liaw, Leaf Yeh, Ming-Jang Lin, and Chrong Jung Lin, "Pinch-off Voltage-Adjustable High-Voltage Junction field-effect transistor," *IEEE Elec. Dev. Lett.*, vol. 28, Aug. 2007, pp. 737–739. (Remark: 7)

[8] G. Massobrio, and P. Antognetti, "Semiconductor Device Modeling with SPICE," 2nd ed., McGraw-Hill, 1998. (Remark: 8)

[9] Elisa Platania, Zhiyang Chen, Filippo Chimento, Alexander E. Grekov, Ruiyun Fu, Liqing Lu, Angelo Raciti, Jerry L. Hudgins, H. Alan Mantooth, David C. Sheridan, J. Casady, and Enrico Santi, "A physics-based model for a SiC JFET accounting for electric-field-dependent mobility," *IEEE Transactions on Industry Applications*, vol. 47, no. 1, 2011, pp. 199–211. (Remark: 7)

[10] M.-D. Ker, H.-C.Hsu, and J.-J. Peng, "Novel implantation method to improve machine-model electrostatic discharge robustness of stacked N-Channel Metal-Oxide Semiconductors (NMOS) in sub-quarter-micron complementary metal-oxide semiconductors (CMOS) technology,"*Japanese Journal of Applied Physics*, Vol. 41, Nov. 2002, pp. L1288-1290. (Remark: 9)

[11] K. Chatty, D. Alvarez, R. Gauthier, C. Russ, M. Abou-Khalil, and B. J. Kwon, "Process and design optimization of a protection scheme based on NMOSFETs with ESD implant in 65nm and 45nm CMOS technologies," *in 29th Electrical Overstress/Electrostatic Discharge Symposium*, 2007, pp. 7A.21–7A.210. (Remark: 6)

Correct References

[1] M. H. Na, E. J. Nowak, W. Haensch, and J. Cai, "The effective drive current in CMOS inverters," in *Int. Electron Devices Meeting (IEDM) Tech. Dig.*, Dec. 2002, pp. 5.4.1–5.4.4.

[2] D. Chang, M. Lee, D. Chen, and V. Liva, "Power junction FETs (JFETs) for very low-voltage applications," in *Proc. Applied Power Electronics Conference and Exposition (APEC)*, 2005, pp. 1419–1423.

[3] M. Kumar, M. Kumar, A. Kumar, A. Das, A. K. Jaiswal, G. Nigam, and K. P. Pandey, "An improved device consideration for ultra-low power applications in junction field effect transistor," *Int. Journal of Emerging Technology and Advanced Engineering (IJETAC)*, vol. 3, no. 2, pp. 292–295, Feb. 2013.

[4] S. Ono, Y. Yamaguchi, Y. Kawaguchi, and A. Nakagawa, "30V sub-micron shallow junction planar-MOSFET for DC–DC converters," in *Proc. Int. Symp. Power Semicond. Devices ICs (ISPSD)*, 2004, pp. 401–404.

[5] T. V. Meenu and R. Komaragiri, "A vertical JFET with improved on to off current performance," in *Proc. Annual Int. Conf. on Emerging Research Areas and Int. Conf. on Microelectronics, Communications and Renewable Energy (AICERA/ICMiCR)*, 2013, pp.1–5.

[6] C. Chiang, P.-C. Chang, P.-S. Tseng, P.-Y. Lai, T.-H. Tang, and K.-C. Su, "Optimization of PESD implant design for ESD robustness of 5V drain-back N-LDMOSFET," in *Proc. Int. Reliability Physics Symp. (IRPS)*, 2016, pp. EL-3-1–EL-3-4.

[7] C.-W. Liaw, L. Yeh, M.-J. Lin, and C. J. Lin, "Pinch-off voltage-adjustable high-voltage junction field-effect transistor," *IEEE Electron Device Letters*, vol. 28, no. 8, pp. 737–739, Aug. 2007.

[8] G. Massobrio and P. Antognetti, *Semiconductor Device Modeling with SPICE*, 2nd ed., New York, USA: McGraw-Hill, 1998.

[9] E. Platania, Z. Chen, F. Chimento, A. E. Grekov, R. Fu, L. Lu, A. Raciti, J. L. Hudgins, H. A. Mantooth, D. C. Sheridan, J. Casady, and E. Santi, "A physics-based model for a SiC JFET accounting for electric-field-dependent mobility," *IEEE Transactions on Industry Applications*, vol. 47, no. 1, pp. 199–211, Jan. 2011.

[10] M.-D. Ker, H.-C. Hsu, and J.-J. Peng, "Novel implantation method to improve machine-model electrostatic discharge robustness of stacked N-channel metal-oxide semiconductors (NMOS) in sub-quarter-micron complementary metal-oxide semiconductors (CMOS) technology," *Japanese Journal of Applied Physics (JJAP)*, vol. 41, pp. L1288–L1290, Nov. 2002.

[11] K. Chatty, D. Alvarez, R. Gauthier, C. Russ, M. Abou-Khalil, and B. J. Kwon, "Process and design optimization of a protection scheme based on NMOSFETs with ESD implant in 65nm and 45nm CMOS technologies," in *Proc. Electrical Overstress/Electrostatic Discharge Symp. (EOS/ESD)*, 2007, pp. 7A.2-1–7A.2-10.

Section II: Important Remarks

Remark:1. IEDM notification in reference must be with "technical digest". The correct way of writing for IDEM papers in listing reference is "in *Int. Electron Devices Meeting (IEDM) Tech. Dig.*," Page numbers must be mentioned as eg. pp. 5.4.1–5.4.4 instead of pp. 541–544.

Remark:2. The whole title of paper listed in the reference, should not with the capital letter at each word. Title name of paper must have to follow this nomenclature: "Power junction FETs (JFETs) for very low-voltage applications" instead of "Power Junction FETs (JFETs) For Very Low-Voltage Applications". Conference paper in reference should not have vol. and issue.

Remark:3. For longer names and 3 or more numbers of authors must "abbreviate authors name" instead of writing full authors name. Issue must replace by "no." along with "vol. and page no. of published article. To use any Journals/Periodicals in reference must follow IEEE reference listing style (Authors name, Tital name, *Publication*, Vol., no., Page no., Year.).

Remark:4. No need to use location in reference for conference Proceedings (published) papers. If paper is unpublished then only "place of conference" needed to be mention in citied references. Detail differences are listed in section III (IEEE FORMAT)

Remark:5. Wrong format for conference paper, all author's name should be abbreviate, not just one. For any cited references for books, conferences, periodicals must use similar way to list their authors name.

Remark:6. Wrong format for conference paper. Must checkout correct page no. from corresponding conference paper, few conferences use to write page no. with capital alphabet letter. For a paper published in IRPS conference, the correct way of writing in listing reference is "in *Proc. Int. Reliability Physics Symp. (IRPS)"*.

Remark:7. Wrong format for journal paper. Tital name should not with start with the capital letter at each word for listing reference. In this case, it should be "Pinch-off voltage-adjustable high-voltage junction field-effect transistor" instead of "Pinch-off Voltage-Adjustable High-Voltage Junction field-effect transistor". Must abbreviate author's name and use number (no.) with vol.

Remark:8. Wrong format for book. Books in listing reference must follow IEEE format (Authors name, *Book name*, Publications, Edition, Vol., Place, Year, Page no.).

Remark:9. Wrong format for journal paper. Must need to follow IEEE format for listing reference style (Authors name, Tital name, *Publication*, Vol., no., Page no., Year.). Page no. use to start with capital letter alphabets for *Japanese Journal of Applied Physics* eg. "pp. L1288–L1290".

- Must need to be careful about spacing between words, comma-word, and abbreviated authors names.
- Every source listed in our references should be accessible in detail by others who read our work. We must need to think of it as "a trail of breadcrumbs" that we leave for readers to show them where they can go to find the original source material for themselves.

Section III: IEEE FORMAT

A numbered list of references must be provided at the end of the paper. The list should be arranged in the order of citation in text, not in alphabetical order. List only one reference per reference number.

In text, each reference number should be enclosed by square brackets. Citations of references may be given simply as "in [1] ...", rather than as "in reference [1] ...".
Sample correct formats for various types of references are as follows:

Books: (Authors name, *Book name*, Publications, Edition, Vol., Place, Year, Page no..)
[1] G. O. Young, "Synthetic structure of industrial plastics," in *Plastics*, 2nd ed., vol. 3, J. Peters, Ed. New York: McGraw-Hill, 1964, pp. 15–64.
[2] W.-K. Chen, *Linear Networks and Systems*. Belmont, CA: Wadsworth, 1993, pp. 123–135.

Periodicals: (Authors name, Tital name, *Publication*, Vol., Page no., Year.)

[3] J. U. Duncombe, “Infrared navigation—Part I: An assessment of feasibility,” *IEEE Trans. Electron Devices*, vol. ED-11, pp. 34–39, Jan. 1959.
[4] E. P. Wigner, “Theory of traveling-wave optical laser,” *Phys. Rev.*, vol. 134, pp. A635–A646, Dec. 1965.

Articles from Conference Proceedings (published): (Authors name, Tital name, *Publication*, Year, Page no..)
[5] D. B. Payne and J. R. Stern, “Wavelength-switched passively coupled single-mode optical network,” in *Proc. IOOC-ECOC*, 1985, pp. 585–590.

Papers Presented at Conferences (unpublished): (Authors name, Tital name, Publication, Place, Date, Year.)
[6] D. Ebehard and E. Voges, “Digital single sideband detection for inter-ferometric sensors,” presented at the 2nd Int. Conf. Optical Fiber Sensors, Stuttgart, Germany, Jan. 2-5, 1984.

Standards/Patents: (Authors name, Tital name, Patent No., Date, Year.)
[7] G. Brandli and M. Dick, “Alternating current fed power supply,” U.S. Patent 4 084 217, Nov. 4, 1978.

Technical Reports: (Authors name, Tital name, Report Publication, Place, TR No., Year.)
[8] E. E. Reber, R. L. Mitchell, and C. J. Carter, “Oxygen absorption in the Earth’s atmosphere,” Aerospace Corp., Los Angeles, CA, Tech. Rep. TR-0200 (4230-46)-3, Nov. 1968.